US009543435B1

(12) **United States Patent**
Basker et al.

(10) **Patent No.: US 9,543,435 B1**
(45) **Date of Patent: Jan. 10, 2017**

(54) **ASYMMETRIC MULTI-GATE FINFET**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/887,384**

(22) Filed: **Oct. 20, 2015**

(51) **Int. Cl.**

H01L 29/735	(2006.01)
H01L 29/78	(2006.01)
H01L 29/66	(2006.01)
H01L 29/423	(2006.01)
H01L 29/417	(2006.01)

(52) **U.S. Cl.**
CPC ***H01L 29/7835*** (2013.01); ***H01L 29/41791*** (2013.01); ***H01L 29/42392*** (2013.01); ***H01L 29/6656*** (2013.01); ***H01L 29/66545*** (2013.01); ***H01L 29/66659*** (2013.01); ***H01L 29/66795*** (2013.01); ***H01L 29/785*** (2013.01); *H01L 2029/7858* (2013.01)

(58) **Field of Classification Search**
CPC H01L 29/7835; H01L 29/42392; H01L 29/41791; H01L 29/6656; H01L 29/785; H01L 29/66795; H01L 29/6645; H01L 29/66659
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,344,396	B1	2/2002	Ishida et al.	
6,794,256	B1	9/2004	Fuselier et al.	
7,772,048	B2 *	8/2010	Jones	H01L 21/84 257/E21.205
7,863,136	B2	1/2011	Goldbach et al.	
8,618,616	B2	12/2013	Pham	

(Continued)

OTHER PUBLICATIONS

Basker et al., "Asymmetric Multi-Gate Finfet", U.S. Appl. No. 14/949,964, filed Nov. 24, 2015.

(Continued)

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(57) **ABSTRACT**

An asymmetrical finFET device includes at least one semiconductor fin on an upper surface of a semiconductor substrate. The fin extends along a length of the semiconductor substrate to define a fin length. A plurality of gate structures wrap around the sidewalls and upper fin surface of the fin. The plurality of gate structures includes at least one desired gate structure surrounded by at least one sacrificial gate structure. A first source/drain region is formed adjacent a first sidewall of the at least one desired gate structure, and a second source/drain region is formed adjacent a second sidewall of the at least one desired gate structure opposite the first sidewall. The dimensions of the first and second source/drain regions are asymmetrical with respect to one another.

3 Claims, 11 Drawing Sheets